U.S. Patent Application 09/435,154
Specification & Drawings
with pending claims

Proposed Amendment

Please amend claims as follows.

1. **(Thrice Amended)** A ferroelectric liquid crystal display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surface of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, [a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region] a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and [a third impurity region being in contact with said second channel formation region] second source and drain regions,

wherein [said first impurity region of said n-channel TFT is disposed so as to partially overlaps with a portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein [said third impurity region of said p-channel TFT is disposed so as to partially overlaps with said portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions.

2. (No Amended) A ferroelectric liquid crystal display device according to claim 1, wherein said first conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

3. (No Amended) A ferroelectric liquid crystal display device according to claim 1, wherein each of said first conductive layers of said n-channel TFT and said p-channel TFT comprises a single layer or a plurality of layers.

4. (No Amended) A ferroelectric liquid crystal display device according to claim 1, wherein said second conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

5. **(Amended)** A ferroelectric liquid crystal display device according to claim 1,

wherein said [first impurity region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region] semiconductor layer of said p-channel TFT has no LDD regions.

6. **(Twice Amended)** A ferroelectric liquid crystal display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surface of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, [a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region] a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and [a third impurity region being in contact with said second channel formation region] second source and drain regions,

wherein [said first impurity region of said n-channel TFT is disposed so as to partially overlaps with a portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein [said second impurity region of said n-channel TFT is disposed so as not to overlaps with said second conductive layer] the portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT does not overlap said second source and drain regions;

wherein [said third impurity region of said p-channel TFT is disposed so as to partially overlaps with said portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions.

7. (No Amended) A ferroelectric liquid crystal display device according to claim 6, wherein said first conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

8. (No Amended) A ferroelectric liquid crystal display device according to claim 6, wherein each of said first conductive layers of said n-channel TFT and said p-channel TFT comprises a single layer or a plurality of layers.

9. (No Amended) A ferroelectric liquid crystal display device according to claim

6, wherein said second conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

10. **(Amended)** A ferroelectric liquid crystal display device according to claim 6, wherein said [first impurity region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region] semiconductor layer of said p-channel TFT has no LDD regions.

11. **(Twice Amended)** A ferroelectric liquid crystal display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region;

wherein said [first impurity region is disposed so as to partially overlaps with said first gate electrode] first gate electrode partially overlaps said first impurity region, and

said p-channel TFT comprising:

a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film, said second semiconductor layer comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein [said third impurity region is disposed so as to partially overlaps with said second gate electrode] second gate electrode partially overlaps said third impurity region, and

wherein a wiring is [electrically] connected to said third impurity region.

12. **(Amended)** A ferroelectric liquid crystal display device according to claim 11, wherein said first and second gate electrodes comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

13. (No Amended) A ferroelectric liquid crystal display device according to claim 11, wherein said first impurity region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region.

14. **(Twice Amended)** A goggle type display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT

having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surface of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, [a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region] a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and [a third impurity region being in contact with said second channel formation region] second source and drain regions,

wherein [said first impurity region of said n-channel TFT is disposed so as to partially overlaps with a portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein [said third impurity region of said p-channel TFT is disposed so as to partially overlaps with said portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT is partially overlaps said second source and drain regions.

15. (No Amended) A goggle type display device according to claim 14, wherein said first conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

16. (No Amended) A goggle type display device according to claim 14, wherein each of said first conductive layers of said n-channel TFT and said p-channel TFT comprises a single layer or a plurality of layers.

17. (No Amended) A goggle type display device according to claim 14, wherein said second conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

18. (**Amended**) A goggle type display device according to claim 14, wherein said [first impurity region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region] semiconductor layer of said p-channel TFT has no LDD regions.

19. (**Twice Amended**) A goggle type display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT

having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surface of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, [a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region] a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and [a third impurity region being in contact with said second channel formation region] second source and drain regions,

wherein [said first impurity region of said n-channel TFT is disposed so as to partially overlaps with a portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein [said second impurity region of said n-channel TFT is disposed so as not to overlaps with said second conductive layer] the portion which said second conductive layer is in contact with said gate insulating film in said n-channel region does not overlap said first source and drain regions;

wherein [said third impurity region of said p-channel TFT is disposed so as to partially overlaps with said portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlap said second source and drain regions.

20. (No Amended) A goggle type display device according to claim 19, wherein said first conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

21. (No Amended) A goggle type display device according to claim 19, wherein each of said first conductive layers of said n-channel TFT and said p-channel TFT comprises a single layer or a plurality of layers.

22. (No Amended) A goggle type display device according to claim 19, wherein said second conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

23. (**Amended**) A goggle type display device according to claim 19, wherein said [first impurity region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region] semiconductor layer of said p-channel TFT has no LDD regions.

24. (**Twice Amended**) A goggle type display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region;

wherein said [first impurity region is disposed so as to partially overlaps with said first gate electrode] <u>first gate electrode partially overlaps said first impurity region</u>, and

said p-channel TFT comprising:

a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film, said second semiconductor layer comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said [third impurity region is disposed so as to partially overlaps with said second gate electrode] <u>second gate electrode partially overlaps said third impurity region</u>, and

wherein a wiring is [electrically] connected to said third impurity region.

25. (**Amended**) A goggle type display device according to claim 24, wherein said first and second gate electrode<u>s</u> comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

26. (No Amended) A goggle type display device according to claim 24, wherein said first impurity region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region.